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REMARKS

I. AMENDMENT TO THE SPECIFICATION

Applicants have amended paragraph [37] on page 11 to correct an obvious typographical error.

II. AMENDMENT TO THE CLAIMS

For clarification, Applicants have cancelled claims 2, 4, 10, 11, and 16-19, amended claims 1, 3, 5, 8-9, and 20-26, and added new claims 27-34. In the following discussion, these amendments and new claims will be grouped into families of independent claims, with remarks concerning each new or amended independent claim, followed by its new or amended direct and indirect dependent claims.

Independent Claim 1 and Dependents: Amended and New

Independent claim 1 has been amended to recite a method for making a transistor containing a gate dielectric structure, comprising providing a gate conductor; providing a channel; and providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process. Support for this claim is clearly found in FIG. 1 and associated description in paragraphs [20] through [32], and in FIG. 2a and FIG. 2b and associated description in paragraphs [33] through [38].

FIG. 1 and associated description in paragraphs [20] through [32] support new claim 27, which recites the method of claim 1 wherein the transistor is a SONOS transistor. Claim 20 has been amended to depend from claim 27, with specific support in paragraphs [29] to [31]. New claim 34 also depends from claim 27, with specific support in paragraph [22].

FIG. 2a and FIG. 2b and associated description in paragraphs [33] through [38] support claim 3, which has been amended to recite the method of claim 1 wherein the transistor is a thin film transistor. Claim 5 has been amended to depend from new claim 3, with specific support in paragraph [37]. New claim 29, which depends from claim 3, is further supported by paragraph [33]. FIG. 1 and associated description in paragraphs [20] through [32], and in paragraph [33], support new claim 28, which recites the method of claim 3 wherein the transistor is a SONOS transistor. Claim 8 has been amended to depend from claim 28.

Independent Claim 9: Amended

Independent claim 9 has been amended to recite a method for making a SONOS device, comprising providing a channel region; providing a first oxide layer on the channel region by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer. Support for this claim is found in FIG. 1 and associated description in paragraphs [20] through [32].

Independent Claim 21 and Dependents: Amended and New

Support is found in FIG. 1 and associated description in paragraphs [20] through [32] for independent claim 21, which has been amended to recite a method for making a gate dielectric structure for a SONOS device, comprising providing silicon (paragraph [20]); providing an oxide layer of a gate dielectric structure on the silicon by in-situ steam generation, the oxide layer having a thickness of about 10 to about 200 angstroms; and annealing the oxide layer in a nitric oxide atmosphere. New claim 30 recites the method of claim 21, wherein the silicon is a surface of a silicon wafer (paragraph [20]),

while new claim 31 recites the method of claim 21, wherein the silicon comprises polysilicon (paragraph [20].)

Independent Claim 22: Amended

Independent claim 22 has been amended to recite a method for making a gate dielectric structure for a thin film transistor or a SONOS device, comprising providing a gate conductor; providing a channel region; and providing, between the gate conductor and the channel region, an oxide layer of a gate dielectric structure by an in-situ steam generation process (support from FIGs 1, 2a, 2b and paragraphs [20]-[38]) performed at a temperature ranging from about 600 (paragraph [37]) to about 1050 (paragraph [26]) degrees Celsius, a pressure ranging from about 100 millitorr to about 760 torr (paragraph [25]), and for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms (paragraph [28].)

Independent Claim 23 and Dependents: Amended and New

Independent claim 23 has been amended to recite a thin film transistor containing a gate dielectric structure made by a method comprising providing a gate conductor; providing a channel region; and providing, between the gate conductor and the channel region, an oxide layer of the gate dielectric structure on the channel region by an in-situ steam generation process, with support from FIG. 2a and FIG. 2b and associated description in paragraphs [33] through [38]. Depending from claim 23 is new claim 32, wherein the transistor of claim 23 comprises a floating gate (see paragraph [33].)

Independent Claim 24: Amended

Independent claim 24 has been amended to recite a SONOS semiconductor device made by a method comprising providing a channel region; providing a first oxide layer

on the channel region by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer. Support appears in FIG. 1 and associated description in paragraphs [20] through [32].

Independent Claim 25 and Dependents: Amended and New

Independent claim 25 has been amended to recite an integrated circuit containing a thin film transistor with a gate dielectric structure made by a method comprising providing a gate conductor; providing a channel; and providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process, with support in FIG. 2a and FIG. 2b and associated description in paragraphs [33] through [38]. New claim 33 recites the integrated circuit of claim 25 wherein the transistor comprises a floating gate (see paragraph [33].)

Independent Claim 26: Amended

Independent claim 26 has been amended to recite an integrated circuit containing a SONOS semiconductor device made by a method comprising providing a silicon wafer or silicon layer; providing a first oxide layer on the silicon wafer or silicon layer by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer, as described in FIG. 1 and associated description in paragraphs [20] through [32].

III. CLAIM REJECTIONS

Independent claims 1, 16, 23 and 25 were rejected under 35 USC 103(a) as unpatentable over Noguchi et al., U.S. Patent No. 6,190,949, in view of pre-grant patent publication Kusumi et al., Publication No. 2002/0039822. Claims 8, 15, 20, and 22 were rejected under 35 USC 103(a) as unpatentable over Noguchi et al. and Kusumi et al. in

view of US. Patent No. 6,362,085 to Yu et al. Independent claims 9, 24, and 26 were rejected under 35 USC 103(a) as unpatentable over U.S. Patent No. 5,324,675 to Hayabuchi in view of Kusumi et al.

A. Claim Rejection 35 US 103, Claims 1, 16, 23, and 25

Independent claims 1, 16, 23, and 25 have been rejected under 35 USC 103(a) as being unpatentable over Noguchi et al. in view of Kusumi et al.

Regarding the rejection of claim 1: As amended, claim 1 recites a method for making a transistor containing a gate dielectric structure, comprising: providing a gate conductor; providing a channel; and providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process.

argue This claim clearly distinguishes over Noguchi et al., which makes no use of an in-situ steam generation process. The claim similarly distinguishes over Kusumi et al., as shown in FIG. 54H. Formation of oxide regions in the twelfth embodiment, cited by the Examiner, is the same as in the first embodiment (paragraph [0526].) Although an in-situ argue steam generation process was known to Kusumi et al., the oxide layer 28 between the gate conductor 31A and the channel region (not labeled, but located in the semiconductor substrate 21 between source 42 and drain 43) was not created by an in-situ steam generation process. Oxide layer 28 is formed by thermal oxidation in an oxygen atmosphere (paragraph [0161].) As the in-situ steam generation process is not used in the analogous oxide layer (23 in Noguchi et al., 28 in Kusumi et al.) in either reference, clearly the references cannot be combined to teach or suggest using this method to create the oxide of the present invention.

Regarding the rejection of claim 16, claim 16 has been cancelled.

Regarding the rejection of claim 23, claim 23 has been amended to recite a thin film transistor containing a gate dielectric structure made by a method comprising: providing a gate conductor; providing a channel region; and providing, between the gate conductor and the channel region, an oxide layer of the gate dielectric structure on the channel region by an in-situ steam generation process. This claim clearly distinguishes over both Noguchi et al. and Kusumi et al. for the reasons described for claim 1.

Regarding the rejection of claim 25, claim 25 has been amended to recite an integrated circuit containing a thin film transistor with a gate dielectric structure made by a method comprising: providing a gate conductor; providing a channel; and providing, between the gate conductor and the channel, an oxide layer of the gate dielectric structure by an in-situ steam generation process. This claim also clearly distinguishes over both Noguchi et al. and Kusumi et al. for the reasons described for claim 1.

B. Claim Rejection 35 US 103, Claims 8, 15, 20, and 22

Claims 8, 15, 20, and 22 have been rejected under 35 USC 103(a) as being unpatentable over Noguchi et al. and Kusumi et al. and further in view of Yu et al.

Regarding the rejection of claim 8, this claim depends indirectly from claim 1, (by way of claim 28 and claim 3) and thus distinguishes over the combination of Noguchi et al. and Kusumi et al. for the reasons described in section A. Even if the clear distinction described earlier did not exist, Applicants respectfully suggest there is no motivation to combine Yu et al. with Noguchi et al. and Kusumi et al. as proposed by the Examiner. Yu et al. describe that it is desirable to incorporate nitrogen in the gate oxide to increase the dielectric and hot carrier resistance (column 1, lines 49-55.) Immediately after this

description, however, Yu et al. describe that "undesirable side effects were encountered" in incorporating the nitrogen into the gate oxide layer (column 1, lines 56-57.) Such undesirable side effects, however, would have discouraged – rather than encouraged – the skilled artisan to make the proposed modification.

Further, the gate oxides mentioned in Yu et al. are about 500 angstroms thick, much thicker than the oxide layers of 200 angstroms or less described in the present invention (paragraphs [28] and [36]); in fact Yu et al. speak of "relatively thick (500.ANG.) gate oxides" (column 1, line 54.) The difference in character of the oxide layers of Yu at al. and the present invention also teaches away from applying the same techniques.

Regarding the rejection of claim 15, this claim depends from claim 9, which is discussed in the section C. For the reasons noted in remarks directed to the rejection of claim 8, though, one skilled in the art would have no motivation to combine the references as suggested by the Examiner.

Regarding the rejection of claim 20, this claim depends from claim 27, which depends from claim 1, and thus distinguishes over the combination of Noguchi et al. and Kusumi et al. for the reasons described in section A, above. Further, as noted in remarks directed to the rejection of claim 8, one skilled in the art would have no motivation to combine the references as suggested by the Examiner.

Regarding the rejection of claim 22, this claim has been amended to recite a method for making a gate dielectric structure for a thin film transistor or a SONOS device, comprising: providing a gate conductor; providing a channel region; and providing, between the gate conductor and the channel region, an oxide layer of a gate

dielectric structure by an in-situ steam generation process performed at a temperature ranging from about 600 to about 1050 degrees Celsius, a pressure ranging from about 100 millitorr to about 760 torr, and for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms. As claim 22 no longer includes any limitation relating to an anneal step, the teachings of Yu et al. no longer apply.

C. Claim Rejection 35 US 103, Claims 9, 24, and 26

Claim 9, 24, and 26 have been rejected as unpatentable over Hayabuchi in view of Kusumi et al. Regarding the rejection of claim 9, this claim has been amended to recite a method for making a SONOS device, comprising: providing a channel region; providing a first oxide layer on the channel region by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer.

The Examiner acknowledges that Hayabuchi does not disclose the use of an in-situ steam generation process. The Examiner asserts that Kusumi et al. "discloses the oxide layer 39 ... formed by an ISSG process [0534]. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use the ISSG oxide 39 layer teaching of Kusumi et al. to replace the oxide layer 23 of Noguchi et al., because it would have created a superior quality oxide layer as taught by Kusumi et al., [0214]."

As Noguchi et al. is not cited as a reference for this rejection, it is presumed that the Examiner intended to refer not to "the oxide layer 23 of Noguchi" but rather to the oxide layer 3 of Hayabuchi in FIG. 6.

Applicants respectfully suggest that the references cannot properly be combined as suggested by the Examiner. Kusumi et al. describe a floating gate device (formation

of the floating gate 40B in FIG. 54H is described in [0535]); Hayabuchi an ONO device (FIG. 6.) These devices operate by different mechanisms: In Kusumi et al., "hot electrons are implanted with high efficiency into the floating gate electrode 40B" (see [0537]), while charge is trapped in SONOS devices by tunneling of charge carriers. The oxide layer 3 of Hayabuchi and the oxide layer 39 of Kusumi et al. serve different roles in different devices. Thus there would be no motivation for one skilled in the art to use the method of Kusumi et al. to create the oxide layer 3 of Hayabuchi.

Further, for suggestion to combine, the Examiner relies on paragraph [0214] of Kusumi et al.. Yet the motivation in the cited paragraph is not applicable to Hayabuchi. In Kusumi et al., the tunnel oxide layer 39 is formed over arsenic-doped n-type silicon [0533]. Paragraph [0214] teaches that when the tunnel oxide layer 39 is formed using an ISSG process:

> "accelerated oxidation of the lightly doped n-type impurity diffusion region 38 doped with the arsenic (As) ions is suppressed and the tunnel insulating film 39 is formed to have a nearly uniform thickness. This prevents an increase in the thickness of the tunnel insulating film 39 and thereby suppresses a reduction in erase speed in the memory element. Since the quality of the tunnel insulating film 39 formed by the internal-combustion thermal oxidation is equal or superior to the quality of a tunnel insulating film formed in an oxygen atmosphere at a temperature of 850 degrees C. or more, the reliability of the memory element is improved."

Clearly the primary reason expressed in Kusumi et al. to use ISSG is not simply to form a superior oxide – in fact Kusumi et al. describe the ISSG oxide as only "equal or superior" – but rather to suppress accelerated oxidation when forming the oxide layer over arsenic-doped silicon. No specific dopant, or in fact any doping at all, is anywhere mentioned in Hayabuchi. Thus no motivation to combine the references exists.

Regarding the rejection of claim 24, this claim has been amended to recite a SONOS semiconductor device made by a method comprising: providing a channel region; providing a first oxide layer on the channel region by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer. For the reasons discussed in the remarks directed to the rejection of claim 9, there is no suggestion to combine the transistor of Hayabuchi and the method of Kusumi et al.

Regarding the rejection of claim 26, this claim has been amended to recite an integrated circuit containing a SONOS semiconductor device made by a method comprising: providing a silicon wafer or silicon layer; providing a first oxide layer on the silicon wafer or silicon layer by an in-situ steam generation process; providing a nitride layer on the first oxide layer; and providing a second oxide layer on the nitride layer. For the reasons discussed in the remarks directed to the rejection of claim 9, there is no suggestion to combine the transistor of Hayabuchi and the method of Kusumi et al.

IV. CONCLUSION

In view of these amendments and remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. **If any objections or rejections remain, Applicants respectfully request an interview to discuss the references.** In such event, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

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Date

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